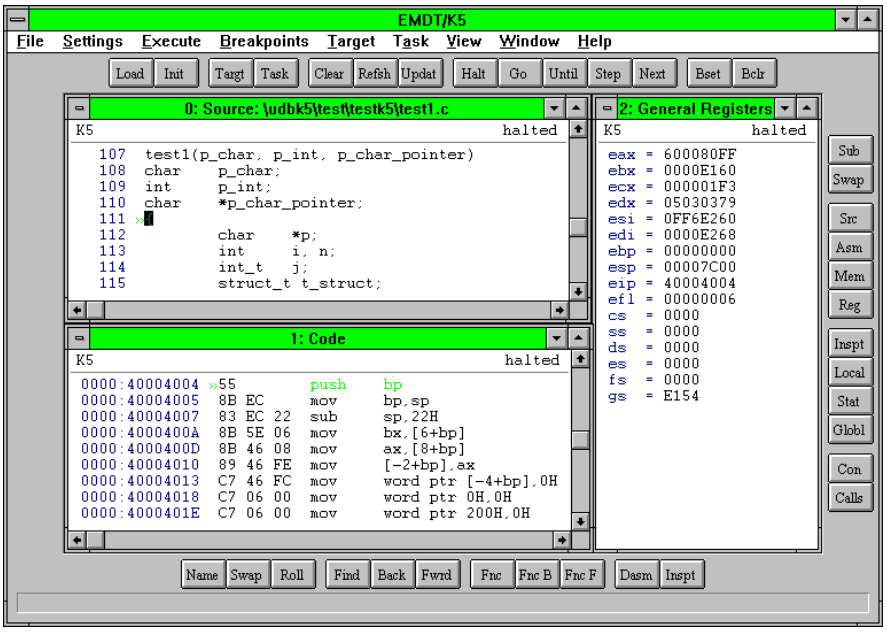
EMDT/K5

Boundary-Scan (JTAG) Emulator for the AMD K5

- **Real-Time Emulation of the AMD K5 Processor**
- **Supports Maximum Processor Clock Speeds with Zero Wait States**
- **Multi-Purpose IEEE-1149.1 (JTAG) Controller**
- **Requires no Hardware or Software Resources from the Target System**
- **Fast Program Download: no need for On-Board ROM.**
- **Examine/Modify Processor Resources Without Imposing Hardware Between the Processor and the Target**
- **Complete Mnemonic Disassembly**
- **User Programmable Toolbars and Complete Macro Facility**
- **On-Line Help System**
- **Optional Trace Capability Using HP 1650/16500/1660 Logic Analyzer with K5 Preprocessor**



Corelis' EMDT/K5 boundary-scan Emulator for the AMD K5 processor introduces a new generation of development tool technology. The EMDT/K5 allows users to debug high-speed, cached applications at the full speed of the target processor. Controlled by the Corelis PC-1149.1/100F ISA (PC) Bus boundary-scan Controller Board, the EMDT/K5 offers the user a tool with a powerful feature set at a fraction of the cost of traditional in-circuit emulators. The EMDT/K5 is supplied with a "true" Microsoft Windows™ user interface.

The HP1650/16500/1660 logic analyzer when combined with a matching preprocessor interface and software, eliminates the need for individual probe lead connection, and adds additional real-time debug capabilities to the K5. Some of the capabilities are: capture of real-time K5 mnemonic disassembly with time stamping, pre-defined complex triggering for address, data and control sequences, timing and state measurements, address range qualification, display of cycle status information and Software Performance Analysis (SPA).

Overview

The Corelis EMDT/K5 utilizes the industry standard IEEE-1149.1 (JTAG) Boundary Scan Test port to access the internal debug resources available on the AMD K5 processor. Since the boundary-scan logic of the processor is separate from the core processor logic itself, this access mechanism allows complete non-intrusive access to any processor resources. Thus, no interrupts, no RAM, ROM or registers need to be assigned for debug purposes and no ROM based debugger or loader program is required. At the same time, no peripheral resources such as serial ports are needed to communicate with the emulator/debugger.

In additional to these benefits, the use of the JTAG interface also ensures that processor access is maintained even when the processor 'hangs' or otherwise runs out of control.

Programs and data can be downloaded to any part of the system RAM through the JTAG port without the need for a resident loader program.

The JTAG interface is a simple, 13-wire interface that connects to the target system via a flexible ribbon cable, and does not require the removal of the microprocessor. Most other emulators require connection of a bulky, fragile pod that requires removing the microprocessor from the target system. The JTAG interface is controlled by a Corelis developed boundary-scan controller board that can be easily installed into a PC in an ISA bus slot. Figure 1 shows the system configuration of a typical EMDT/K5 development system.

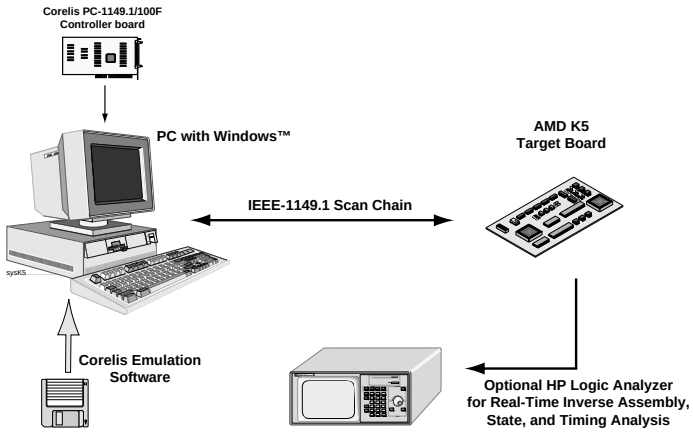


Figure 1. Typical K5 Development System

Real-Time Analysis

Due to the nature and the low cost of the emulator hardware, a real-time trace of processor activity is not provided on the EMDT/K5. However, this capability can be added by using a HP1650/16500/1660 logic analyzer in combination with a K5 preprocessor. Addition of a logic analyzer augments the debugger system with the following capabilities :

- Real-Time Disassembly of instructions, operands, and I/O operations
- State trace of address, data and control lines
- Timing and state mode measurements
- Selective recording of address ranges
- Predefined triggering for address, data and control sequences
- Software Performance Analysis (SPA)

Contact your local Hewlett Packard sales office for additional information.

Emulator Functions

The EMDT/K5 is completely transparent, requires no target system memory or I/O space, no interrupts and no target resident monitor or loader code. Supported functions include :

- Reset processor
- Set breakpoints
- Start and stop the processor
- Single Step
- Display and modify processor registers
- Display and modify memory
- Read and write to processor
- Disassembly memory using K5 mnemonics
- Download code

In addition to all the features mentioned above, the EMDT/K5 is the only hardware/software non-intrusive emulator available on the market. There is no electrical loading of the AMD K5 signals, no linking of the user program to a traditional emulator monitor is required, and no wait states are inserted. The EMDT/K5 is also significantly less expensive than other existing CISC/RISC processors' emulators.

User Interface

The Corelis EMDT/K5 user interface, shown in figure 2, was designed for usability and as such

is the most intuitive debugger available for embedded systems debugging. With a powerful macro language, the interface can be customized to work like your favorite editor or debugger, hence it works like you do. Powerful macro sequences can be bound to toolbar buttons, keys, breakpoints, and other debugging events. The user interface allows a developer to clearly see the application being debugged.

Target Connector

The EMDT/K5 emulator connects to the K5 target via a 26-pin, two row header type connector. The header is made out of two (2) rows of 13 pins, each pin is a 0.025" x 0.025" square post and the spacing between adjacent pins and between the two rows is 0.100". The header pin assignment is illustrated as shown in figure 3.

Boundary-Scan Test

Boundary-scan, as defined in the IEEE-1149.1 standard, is an integrated method for testing interconnects on printed circuit boards and is implemented at the IC level by the semiconductor manufacturer. In a boundary-scan IC, the core logic in the chip is surrounded by a shift register stage comprised of a number of boundary-scan cells. The boundary-scan cells allow you to observe what is happening at the inputs of the device and to control the state of the outputs of the device. All of this is controlled through 5 defined signals (4 mandatory) on the component.

Corelis offers a wide range of software products for boundary-scan testing that are compatible with the K5 JTAG controller card, including an Automatic boundary-scan Test Program Generator (ATPG) for automatic interconnect

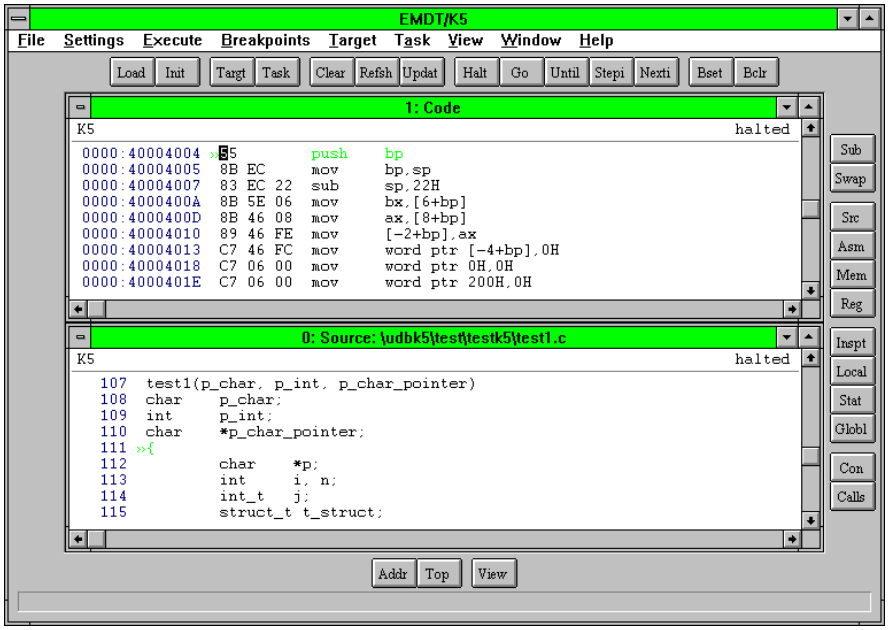
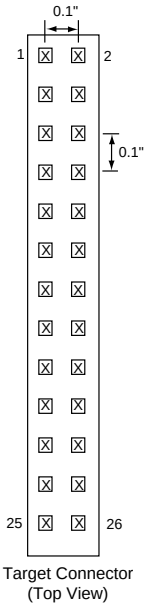


Figure 2. User Interface



Target Connector
(Top View)

Header Pin	AMD K5™ Direction	AMD K5™ Signal Name
1	IN	TRST*
3	IN	TDI
5	OUT	TDO
7	IN	TMS
9	IN	TCK
11	IN	R/S*
13	IN	System Reset[1]
15	IN	RESET
17	OUT	Spare Output
19	IN	INIT
21	OUT	PRDY
23	OUT	/SMIACT
25	IN	Spare Input

[1]System Reset controls a switch on the target adapter pod that can be connected to the target's global reset.

Figure 3. Target Connector

test pattern generation and boundary-scan Diagnostics for enhanced fault diagnosis. These products can be used interactively through a Windows-based graphical user interface or directly from the command line.
In addition to using the boundary-scan interface to support interconnect testing, many component manufacturers now provide logic devices such as the AMD MACH family, which can also be programmed through the boundary-scan interface. Using PLD programming software, these devices can now be programmed while in-circuit, even if the device is connected in a boundary-scan chain containing any mixture of boundary-scan compatible components from different manufacturers. The CPLD programming software also provides test capabilities to verify proper operation of the boundary-scan chain prior to programming.

Corelis' JTAG tools provide a total JTAG product life cycle support as depicted in figure 4. Corelis is one of the leaders in lower cost boundary-scan test tools and JTAG emulation. By using the EMDT/K5 JTAG controller and Corelis' boundary-scan interconnect test tools and device programming tools, the K5 JTAG controller board can be used to perform interconnect testing, in-circuit programming of JTAG programmable logic devices, (including AMD MACH devices), and in-circuit emulation. Using the K5 JTAG controller as a host for boundary-scan tools and in-circuit emulation allows hardware and software integrators to take full advantage of the capabilities of the JTAG controller card.

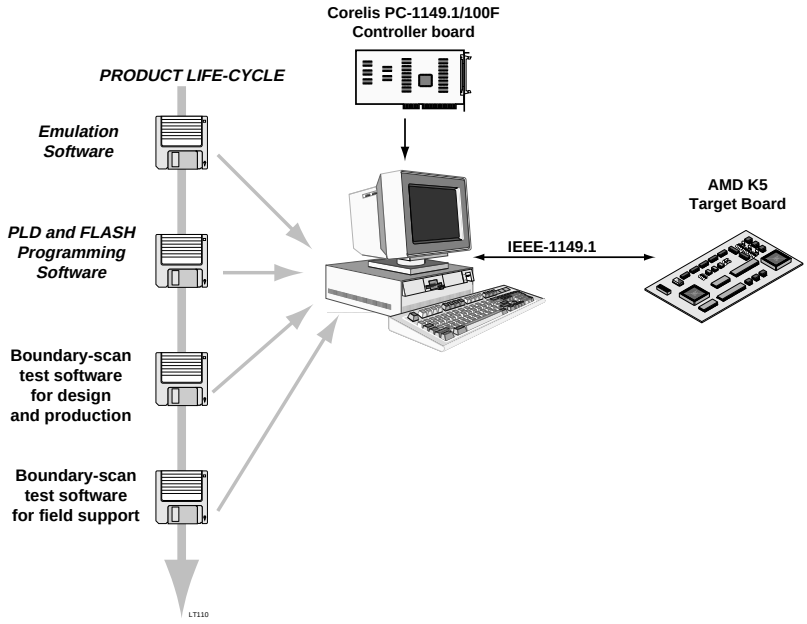


Figure 4. Total JTAG Life-Cycle Support

Ordering Information

EMDT/K5 Emulator

Included :

- Emulation Source Level Debugger on 3.5" Disk
- PC-1149.1/100F JTAG controller card
- JTAG Port connector flatcable to target system
- User's Manual

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